



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,667	03/10/2004	Jae-Hyung Lee	SAM-0528	4158

7590

01/12/2006

Anthony P. Onello, Jr.
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER

NGUYEN, VIET Q

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/797,667

Applicant(s)

LEE ET AL.

Examiner

Viet Q. Nguyen

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Election filed on 12/14/2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 5-8 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-16 is/are allowed.
- 6) ☒ Claim(s) 1,3,4,9,11 and 12 is/are rejected.
- 7) ☒ Claim(s) 2 and 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims **1-4** are preset for examination per applicant's election.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims **1, 3, 4, 9, 11, & 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted **prior art (Fig. 2)** in view of **Choi patent (US 6,272,053 B1)**.

Regarding claim **1 & 9**, Fig. 2 of this application already shows a semiconductor memory circuit in package form (IC 20), which includes at least a plurality of first data IO pads (1DQ), address and instruction pads (ADD, CMD), and second data IO pads, which are all arranged in different groups adjacent to each other. It is noted that Fig. 1 does not teach or suggest that those second IO pads (2DQ) can be selected, configured, and/or selected to be used as either "data IO" pads in first package form" or as "address pad in second package form" as claimed. However, the Choi patent (which also concerns with a similar IO pad arrangement on an IC package including data, address, and other command pads/balls, etc., see **Fig. 5**), further shows that some or a plurality of these pads can be constituted as "**multi-pads**", which could function as "data

Art Unit: 2827

IO” pads in one package form but still could be used as “address” pads in another package form depending on the logic/voltage value of “a control signal” inputted for such IC package. For example, **Fig. 3A** (see col. 3-4) discloses the use of such “multi-pad” that can be programmed and/or discriminated by a specific control signal (address enable, /AE) so that the multi-pad can be configured/used/identified as either “data” or “address” purpose but not both at the same time. Specifically, col. 3 (lines 35-40) stated that ***“...when the address enable signal /AE from an external controller is in low level,... the signals which are inputted into the multi-pad are address signals. On the contrary, when the signal /AE is high level,... the signals inputted into the multi-pad are data signal...”***. Thus, it would be obvious that from this mere suggestion that as some of these multi-pads can be used/programmed differently, and so obviously the whole package, if any, could be appeared from an external user as a different IC package configurations (i.e., **BGA or TSOP**) depending on the external control signals, and thus it can be treated as a whole as a totally different package for use with different users’ purposes possible. Furthermore, one skilled in this art would have been motivated to create such different package/pin configuration by using such programmable “multi-pads” (disclosed by Choi) in combination with the disclosed IO pad grouping arrangement from the applicant’s prior art Fig. 2 in order to meet the claim 1 construction easily without any undue hardship, expedient designs, and/or hindsight constructions.

Regarding claims **3-4 & 11-12**, both “**X16 TSOP**” and “**X36 BGA**” package format has already been acknowledged and discussed in this application’s background as

Art Unit: 2827

conventional package structure as well, and do not add further novelty into the structure of claim 1..

4. Claims **2 & 10** are objected as being dependent upon rejected claim 1, however, it contain allowable subject matter over prior arts of record for requiring the use of specific data latches & data buffer together with such control signal of claim 1.


5. Claims **13-16** are allowable over prior arts of record because claim 13 specifically requiring that the multi-pad or **generic pad** can be used as ***instruction pad*** in second package form but the Choi patent is silent with respect to that instruction pad design. choice/construct.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2827

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


V. Nguyen
01/07/2006



VIET Q. NGUYEN
PRIMARY EXAMINER